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EXAMINER
ORTIZ, EDGARDO

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/751,551	Applicant(s) Lian Et.al.
	Examiner Edgardo Ortiz	Art Unit 2815

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Sep 18, 2002*.

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-13 and 21-30* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-13 and 21-30* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to an amendment filed September 18, 2002 on which Applicant amended claim 8 and added new claims 25-30.

Claim Objections

1. Claim 29 is objected to because of the following informalities: the claim discloses a "second conductive liner" where it should read "a conductive oxide". Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-13 and 21-30 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Applicant's admitted prior art, as shown in figure 2 in view of Kotecki (BaSrTiO3 dielectrics for future stacked-capacitor DRAM). With regard to Claim 1, Applicant's admitted prior art teaches a conductive barrier layer (122), a first conductive liner (132) deposited over the conductive barrier layer and a second conductive liner (134) deposited over the first conductive liner, the

second conductive liner comprising a conductive oxide and a conductive layer (124) deposited on the second conductive liner.

However, Applicant's admitted prior art fails to teach that the conductive layer and the first conductive liner comprise the same material. Kotecki teaches a DRAM structure which includes a conductive barrier layer (TaSiN), a first conductive liner (Pt), a dielectric layer (BSTO) and a conductive layer (Pt) deposited over the dielectric layer, wherein the conductive layer and the first conductive liner comprise the same material, in this case Pt. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Applicant's admitted prior art to include a conductive layer and a first conductive liner comprising the same material, as clearly suggested by Kotecki, in order to provide electrodes with good adhesion and improve the electrical conductivity characteristics of the electrode, by the use of platinum group metals such as platinum and iridium.

With regard to Claim 2, Applicant's admitted prior art teaches a layer (134) including second conductive liner that comprise a conductive oxide (IrO2).

With regard to Claims 3, 5, 9 and 11; a further difference between the claimed invention and Applicant's admitted prior art is, the thicknesses of the first and second conductive liners. It would have been an obvious modification to someone with ordinary skill in the art, at the time of

the invention, to modify the structure as taught by Applicant's admitted prior art to include the thickness of the first and second conductive liners as claimed, in order to reduce oxygen diffusion into a conductive layer such as polysilicon below the multi-layer electrode.

With regard to Claims 4 and 10, a further difference between the claimed invention and Applicant's admitted prior art is, the conductive layer and the first conductive liner comprising Pt. Kotecki teaches a DRAM structure which includes a conductive barrier layer (TaSiN), a first conductive liner (Pt), a dielectric layer (BSTO) and a conductive layer (Pt) deposited over the dielectric layer, wherein the conductive layer and the first conductive liner comprise the same material, in this case Pt. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Applicant's admitted prior art to include a conductive layer and a first conductive liner comprising Pt, as clearly suggested by Kotecki, in order to provide electrodes with good adhesion and improve the electrical conductivity characteristics of the electrode, by the use of platinum (precious group) metals such as platinum and iridium.

With regard to Claims 6 and 12, a further difference between Applicant's admitted prior art and the claimed invention is, a conductive barrier layer that comprises TaSiN. Kotecki teaches a conductive layer that comprises TaSiN. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as

taught by Applicant's admitted prior art to include a conductive barrier layer that comprises TaSiN, as clearly suggested by Kotecki, since it is a well known barrier layer material because of its oxidation preventing quality.

With regard to Claims 7 and 13, a further difference between Applicant's admitted prior art and the claimed invention is, an integrated circuit that comprises a DRAM or a FRAM. Kotecki teaches a DRAM structure which includes a conductive barrier layer (TaSiN), a first conductive liner (Pt), a dielectric layer (BSTO) and a conductive layer (Pt) deposited over the dielectric layer. Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to use a multi-layer electrode structure as the one disclosed by Kotecki in a memory device such as a FRAM or DRAM.

With regard to Claim 8, Applicant's admitted prior art teaches a conductive barrier layer (122), a first conductive liner (132) deposited over the conductive barrier layer, a second conductive liver (134) deposited over the first conductive liner, the second conductive liner comprising a conductive oxide (IrO2) and a conductive layer (124) deposited on the second conductive liner.

However, Applicant's admitted prior art fails to show a first conductive liner comprising a molecular grain structure having a plurality of columns and a conductive layer comprising a

molecular grain structure having a plurality of columns, wherein the columns of the conductive layer are not aligned with the columns of the first conductive liner.

Kotecki teaches a DRAM structure which includes a conductive barrier layer (TaSiN), a first conductive liner (Pt), a dielectric layer (BSTO) and a conductive layer (Pt) deposited over the dielectric layer, wherein the first conductive liner and the conductive layer can be deposited by a physical vapor deposition (PVD) process (see Table 1), and as known in the semiconductor art, both first conductive liner and conductive layer would have molecular grain structure having a plurality of columns. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Applicant's admitted prior art to include first conductive liner and a conductive layer comprising Pt, since Pt and Ir are from the same platinum metals group, and having a molecular grain structure having a plurality of columns, wherein the columns of the conductive layer are not aligned with the columns of the first conductive liner, as clearly suggested by Kotecki, in order to improve oxidation resistance.

With regard to Claim 21, Applicant's admitted prior art teaches a second conductive liner (134) that comprise IrO2 or RuO2.

With regard to Claim 23, Applicant's admitted prior art teaches both a conductive layer (124) and a first conductive liner (132) that comprise Pt, Ir, Ru, Pd or combinations thereof.

With regard to Claim 25, a further difference between the claimed invention and the prior art is, a thickness of the second conductive layer so that it can be etched with the same gas used to etch the first conductive liner and the conductive layer. It would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Applicant's admitted prior art to include a thickness of the second conductive layer so that it can be etched with the same gas as claimed, in order to reduce the number of process steps.

With regard to Claim 27, a further difference between the claimed invention and the prior art is, a thickness of the second conductive layer so that it can be etched with the same gas used to etch the first conductive liner and the conductive layer. It would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Applicant's admitted prior art to include a thickness of the second conductive layer so that it can be etched with the same gas as claimed, in order to reduce the number of process steps.

With regard to Claim 28, Applicant's admitted prior art teaches a conductive barrier layer (122), an iridium liner (132) deposited over the conductive barrier layer, a conductive oxide (134)

deposited over the iridium liner and a platinum layer (124) deposited on the second conductive liner.

However, Applicant's admitted prior art fails to show a platinum liner comprising a molecular grain structure having a plurality of columns, a conductive oxide having a thickness of 20-50 angstroms and a platinum layer comprising a molecular grain structure having a plurality of columns, wherein the columns of the conductive layer are not aligned with the columns of the first conductive liner.

Kotecki teaches a DRAM structure which includes a conductive barrier layer (TaSiN), a first conductive liner (Pt), a dielectric layer (BSTO) and a conductive layer (Pt) deposited over the dielectric layer, wherein the first conductive liner and the conductive layer can be deposited by a physical vapor deposition (PVD) process (see Table 1), and as known in the semiconductor art, both first conductive liner and conductive layer would have molecular grain structure having a plurality of columns. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Applicant's admitted prior art to include first conductive liner and a conductive layer comprising Pt, since Pt and Ir are from the same platinum metals group, and having a molecular grain structure having a plurality of columns, wherein the columns of the conductive layer are not aligned with the columns of the first conductive liner, as clearly suggested by Kotecki, in order to

improve oxidation resistance. As for the claimed conductive oxide thickness, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Applicant's admitted prior art to include a thickness of the second conductive layer so that it can be etched with the same gas as claimed, in order to reduce the number of process steps.

With regard to Claim 29, Applicant's admitted prior art teaches a conductive oxide (134) comprising IrO2 or RuO2.

With regard to Claim 30, Applicant's admitted prior art teaches a conductive barrier layer (122), a first conductive liner (132) deposited over the conductive barrier layer and a second conductive liner (134) deposited over the first conductive liner, the second conductive liner comprising a conductive oxide and a conductive layer (124) deposited on the second conductive liner.

However, Applicant's admitted prior art fails to teach the thickness of the second conductive liner. It would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Applicant's admitted prior art to include a thickness of the second conductive layer as claimed, in order to reduce the number of process steps during an etching process.

Response to Arguments

3. Applicant's arguments with respect to claims 8, 22 and 24 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with respect to 1-7, 9-13, 21 and 23 have been fully considered but they are not persuasive. Applicant argues that "Kotecki et.al. do not teach, anticipate or suggest a first conductive liner, as in the Applicant's independent Claim 1". However, the examiner disagrees and notes that the term "liner" is merely a label that does not structurally distinguishes the layer as taught by Kotecki, which clearly suggests the use of a Pt as part of an electrode structure. Additionally, Applicant states that "Kotecki et.al. Teach a 250 nm thick electrode while Applicant's claimed invention (Claim 5), specifically recites a first conductive liner that is 20 to 50 nm thick". The examiner notes that, as stated in the body of the rejection, a modification to the thickness of the first conductive liner as taught by Applicant's admitted prior art, would result in a reduction of oxygen diffusion into a conductive layer below the multi-layer electrode and thus one with ordinary skill would have been motivated to make such a modification. Applicant further argues, that "there is no motivation to combine Kotecki et.al. With the multi-layer electrode of prior art 2". The examiner clearly stated that the motivation to combine Applicant's admitted prior art and Kotecki is provide good adhesion and improve the electrical conductivity characteristics of the electrode, by the use of platinum group metals such as platinum and iridium. Therefore, the claimed invention does not structurally or patentably distinguish from that taught by the prior art and the rejection is maintained.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7722. In case the Examiner can not be reached, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO/AU 2815

11/25/02

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